REMARKS

Claims 1 (as amended) is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The "cutting the plurality of lines if the first exposure regions" at page 8, line 32 to page 9, line 1 of the amendment (Paper No.5) does not find basis in the original disclosure. It is also not clear whether the "cutting" of the first exposure regions with subsequent exposure regions involves double exposure (overexposure) or not. Therefore, this new phrase is considered new matter and is not enabled by the specification. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (Japanese Patent Publication 01-107527) in view of Adair (US Patent 6,184,151). Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent 6,492,073) in view of Adair.

1. Objection of the specification:

The objection of Paper No.4 to the abstract of the disclosure because it had more than 150 words is now withdrawn because a new amended abstract of acceptable length has been received in Paper No.5. However, the amended abstract is still objected to since it has not been submitted on a separate sheet, as requested in the previous Office action (Paper No.4).

Response:

The amended abstract of the disclosure has been re-submitted on a separate sheet as requested in the Office action. Reconsideration of the corrected specification is politely requested.

2. Rejection of claim 1 under 35 U.S.C. 112:

Claim 1 (amended) is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claim 1 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No.5, filed 30 January 2003. In that paper, applicant has stated at page 6, lines 30-31 that "no overexposure areas are formed due to twice exposure", and this statement indicates that the invention is different from what is defined in the claim(s) because the "cutting" of claim 1 reads on crossing or overlapping exposure areas (overexposure areas).

Response:

Claim 1 has been amended for overcoming the rejection of 35 U.S.C. 112. Reconsideration of the currently amended claim 1 is politely requested.

3. Rejection of claims 1-2 under 35 U.S.C. 103(a):

Ueno teaches a method of preventing two-dimensional (optical proximity) effects caused by light diffraction during a photolithography process to form (define) a rectangular (array) pattern. A negative photosensitive resin (photoresist) is formed on a semiconductor substrate. The photoresist is exposed through a first linear mask pattern, 100 (having parallel lines, 101), shown in Figure 1(a). Then the photoresist is exposed through a second linear mask pattern, 200 (having parallel lines, 201), shown in Figure 1(b) and positioned in perpendicular relation to the first exposure pattern to form an array of rectangular unexposed photoresist regions, 400, shown in Figure 2(a).

Ueno does not specify subsequent etching of the substrate using the remaining photoresist pattern as an etching mask and does not specify the formation of storage nodes for a dynamic random access memory (DRAM). Ueno also does not specify that the optical proximity effects to be avoided were corner rounding and pattern shortening.

Adair states that in order to scale down DRAM devices while maintaining sufficient capacitance, corner rounding and shortening effects should be avoided when forming the storage nodes (capacitors) in column 1, at lines 46-53. Adair also teaches plural perpendicular exposures (using masks having parallel linear patterns) of one or more photoresist layers to obtain sharp-edged corners (without significant corner rounding or image shortening) in the resulting photoresist image, followed by etching of an underlying substrate through the remaining photoresist pattern as an etching mask in column 6, at lines 6-50.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the Ueno double exposure method to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by subsequent etching taught by Adair. The expected result of this combination would be to avoid corner rounding and image shortening during DRAM storage node formation.

Response:

The applicant's invention provides a method of forming storage nodes in a DRAM on a semiconductor wafer. The method comprises performing a first exposure process to form **first exposure regions that are lines parallel with each other on the photoresist layer**, and performing a second exposure process to form **second exposure regions that are rectangles**

interlaced with and perpendicular to each other on the photoresist layer, and the second exposure regions doing not overlap the first exposure regions. The first exposure regions and the second exposure regions of the photoresist layer are then removed for forming an array photoresist layer on a thin film layer positioned on the semiconductor wafer. The array photoresist layer functions as a mask to perform an etching process to the thin film layer for forming an array thin film layer as a storage nodes in the DRAM. According to the applicant's invention method, **because the second exposure regions do not overlap the first exposure regions, there is no overexposure area formed by the double exposure processes.**

Ueno (Japanese Patent Publication 01-107527) provides forming method for pattern and eliminating two-dimensional effect due to the diffracting of a light. As shown in the figures, the method uses two photo masks for forming a rectangular pattern, and **the rectangular pattern is defined by crossing parts of the linear mask patterns of the two photo masks.**

Adair (US 6,184,151) provides a method for forming images having sharp corners during lithographic processing and a photomask formed thereby. As shown in Fig.4, the method first forms a blocking layer 120, a hard mask 130 and a photoresist layer 140 on a substrate 112. Then as shown in Fig.5, the method comprises defining patterns of the photoresist layer 140 and **forming a plurality of parallel lines in the hard mask 130**. Another photoresist layer 150 is formed on the substrate 112, as shown in Fig.7, **a plurality of line patterns perpendicular to the lines of the hard mask 130 are defined in the photoresist layer 150**. Finally, an etching process is performed to remove

the blocking layer 120 not covered by the phtoresist layer 150 and the hard mask 130 for exposing portions of the substrate 112.

The combination of Ueno's invention and Adair's invention discloses a double exposure method to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by subsequent etching process, however, **the rectangular array of unexposed photoresist is defined by crossing parts of the linear mask patterns of two photo masks** used in the double exposure method. Consequently, like applicant's admitted prior art, portions of the photoresist layer are exposed twice, forming a plurality of overexposure areas that causes more severe optical proximity effects.

Furthermore, both of the first exposure process and the second exposure process of the combination of Ueno's invention and Adair's invention use **a photo mask including parallel linear patterns to form first exposure regions and second exposures, and the overlap between the first exposure regions and the second exposures form a plurality of overexposure areas.** Comparatively, the first exposure process and the second exposure process of the applicant's method respectively use **a photo mask including parallel linear patterns and a photo mask including rectangle patterns interlaced with and perpendicular to each other to form first exposure regions and second exposure region, and there is no overlap between the first exposure regions and the second exposure regions, therefore,** the formation of overexposure areas is prevented.

In view of the foregoing, applicant believes that the limitations of claims 1-2 of the applicant's invention are

different from the Ueno and Adair. The applicant has amended claim 1 based on the specification (page 9, lines 14-32) for overcoming the rejection, and no new matter is included. Reconsideration of claims 1-2 is politely requested.

4. Rejection of claims 1-2 under 35 U.S.C. 103(a):

Lin teaches a process of microlithography (photolithography) to avoid line end shortening caused by optical proximity effects. Column 6, lines 51-65 describes first exposure of a photoresist through transparent parallel line segments 600 of a first photo mask shown in Figure 18A to form corresponding latent image line segments in the photoresist, then second exposure of end portions of the image line segments in the photoresist with a cutting mask having cutting elements 610 shown in Figure 18B. Lin also states that the order of these exposure steps can be reversed and that these masks and steps can be used equally well for forming images in either positive or negative resists. It should be clear that such cutting of the line segments would also remove other defects at the line ends, such as corner rounding.

Lin does not specify subsequent etching of the substrate using the remaining photoresist pattern as an etching mask and does not specify the formation of storage nodes for a dynamic random access memory (DRAM).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the Lin photolithography method involving a first exposure and second cutting exposure to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by subsequent etching taught by Adair. The expected result of this combination would be to avoid corner rounding and image shortening during DRAM storage node formation.

Response:

The applicant's invention provides a method of forming storage nodes in a DRAM on a semiconductor wafer. The method comprises performing a first exposure process to form **first exposure regions that are lines parallel with each other on the photoresist layer,** and performing a second exposure process to form **second exposure regions that are rectangles interlaced with and perpendicular to each other on the photoresist layer, and the second exposure regions doing not overlap the first exposure regions.** The first exposure regions and the second exposure regions of the photoresist layer are then removed for forming an array photoresist layer on a thin film layer positioned on the semiconductor wafer. The array photoresist layer functions as a mask to perform an etching process to the thin film layer for forming an array thin film layer as a storage nodes in the DRAM. According to the applicant's invention method, **because the second exposure regions do not overlap the first exposure regions, there is no overexposure area formed by the double exposure processes.**

Lin (US Patent 6,492,073) provides a mask set of two masks and a method of using these masks in a double exposure to avoid line shortening due to optical proximity effects. As shown in the figures, a pattern having pattern elements comprising a number of line segments, wherein each of the line segments has one or two free ends which are not connected to other mask pattern elements is to be transferred to a layer of resist. **A first mask is formed by adding line extensions to each of the free ends of the line segments. A cutting mask (second mask) is formed comprising rectangles enclosing each of the line extensions** wherein one of the sides of said rectangles

is coincident with the corresponding free end of said line segment.

Adair (US 6,184,151) provides a method for forming images having sharp corners during lithographic processing and a photomask formed thereby. As shown in Fig.4, the method first forms a blocking layer 120, a hard mask 130 and a photoresist layer 140 on a substrate 112. Then as shown in Fig.5, the method comprises defining patterns of the photoresist layer 140 and **forming a plurality of parallel lines in the hard mask 130.** Another photoresist layer 150 is formed on the substrate 112, as shown in Fig.7, **a plurality of line patterns perpendicular to the lines of the hard mask 130 are defined in the photoresist layer 150.** Finally, an etching process is performed to remove the blocking layer 120 not covered by the phtoresist layer 150 and the hard mask 130 for exposing portions of the substrate 112.

The combination of Lin's invention and Adair's invention discloses a double exposure method to form pattern line elements without line shortening. The method comprises performing a first exposure process which uses a **first mask including line extensions added to each of the free ends of the line segments patterns,** and then performing a second exposure process which uses **a cutting mask (second mask) including rectangle patterns enclosing each of the line extensions so as to cut the ends of the lines to the proper length.**

Comparatively, the applicant's invention discloses a double exposure method to form DRAM storage nodes, and the first exposure process and the second exposure process of the

applicant's method respectively use **a photo mask including parallel linear patterns and a photo mask including rectangle patterns interlaced with and perpendicular to each other to form first exposure regions and second exposure region, and there is no overlap between the first exposure regions and the second exposure regions**, therefore, the formation of overexposure areas is prevented.

In view of the foregoing, applicant believes that the limitations of claims 1-2 of the applicant's invention are different from the Lin and Adair. The applicant has amended claim 1 based on the specification (page 9, lines 14-32) for overcoming the rejection, and no new matter is included. Reconsideration of claims 1-2 is politely requested.

Sincerely yours,

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